IN THE DRAWINGS:

The attached sheet of drawings includes a change to FIG. 28. This sheet, which includes FIGS. 27 through 29, replaces the previous drawing sheet submitted for these figures. In FIG. 28, previously omitted element 207 has been added. (See attached Replacement Sheet and Annotated Sheet Showing Change.)

REMARKS

In the specification, paragraphs **[0006], [0009], [0010], [0017], [0021], [0030]** through **[0032], [0034]** through **[0036], [0039]** and **[0040]** have been amended to correct minor editorial problems. In amended FIG. 28, previously omitted element 207 has been added. No new matter has been added.

The Final Office Action mailed September 22, 2004, has been received and reviewed. Claims 1 through 12 are currently pending in the application.

Claims 5 and 12 have been withdrawn from consideration as being drawn to a non-elected invention. Applicant considers claim 1 to be generic and notes that upon allowance of a generic claim, all claims depending therefrom are also allowable.

Claims 1 through 4 and 6 through 11 stand rejected.

Applicant notes with appreciation the high level of detail and clarity of the final Office Action.

Applicant proposes to amend claims 1 through 4 and 6 through 11. Applicant further proposes to amend withdrawn claims 5 and 12.

The proposed amendments to claims 2 through 12 are solely to enhance antecedent basis and do not surrender, or otherwise affect, the scope of the claims in their prior forms.

Applicant also proposes to add new claims 13 through 15 and respectfully requests reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,726,500 to Duboz et al in View of U.S. Patent No. 6,075,290 to Schaefer et al. and Further in View of U.S. Patent No. 6,441,487 to Elenius et al.

Claims 1 through 4 and 6 through 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,726,500 to Duboz et al.(hereinafter "Duboz") in view of U.S. Patent No. 6,075,290 to Schaefer et al. (hereinafter "Schaefer") and further in view of U.S. Patent No. 6,441,487 to Elenius et al. (hereinafter "Elenius"). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1 through 4 and 6 through 11 are improper because the references, taken alone or in combination, fail to teach or suggest all the claim limitations of the claims (as proposed to be amended) and there is no motivation to combine the references.

Duboz is directed to semiconductor hybrid components, especially linear infrared detectors produced by hybridization. According to one embodiment, a main substrate has integrated thereon active elements which cannot be produced on a silicon substrate, the substrate being made, for example, of AsGa, InP, HgCdTe, or PbTe. Several silicon chips are mounted on the main substrate, by hybridization using indium balls. More specifically, the pads of both integrated components are arranged exactly facing each other and are bonded together by means of indium balls. The hybridization of the two substrates is therefore performed by bonding all the facing contact pads, this bonding establishing both mechanical connection of the two substrates and the electrical connection point by point between each of the photosensitive elements and their respective read circuits. These chips include the read and multiplexing circuits; however, the silicon chips remain of limited size (a few millimeters) so that the thermal stresses (related to a reduction in temperature) are limited, but the detection array may be produced as one piece without butt-joining. It is therefore possible to produce arrays of great length (several centimeters) and of high resolution (at least a thousand points).

Schaefer is directed to chip scale packages having improved package interconnect structures for absorbing thermal stresses (related to an increase in temperature) introduced to bump type contacts on the chip scale packages when attached to an external substrate. According to one disclosed embodiment, a chip scale package 200 comprises a die 202 having a conductive

pad 204 formed thereon that may be coupled to at least one integrated circuit structure (Fig. 2 and col. 5, lines 21-28). A passivation layer 206 is formed on the surface of die 202 and forms a portion of a via 216 that is positioned over conductive pad 204. A resilient protective layer 208 is formed over portions of passivation layer 206 and also forms a portion of via 216 over conductive pad 204. An under bump pad 210 is formed within via 216 and over conductive pad 204. Alternatively, Schaefer indicates that the via portion of protective layer 208 may be offset from the via portion of passivation layer 206, with conductive pad 204 being electrically coupled to under bump pad 210 by a redistribution layer (col. 5, lines 40-44). A contact bump 212 is formed over under bump pad 210 using conventional solder bumping or balling techniques for subsequent reflow to a board contact on an external substrate 214 (col. 6, lines 44-45 and col. 7, lines 8-13).

Elenius et al. describes a chip scale package 8 comprising a semiconductor die formed from a wafer 14 having bond pads 18, 20 located proximate to an outer perimeter 21 of the semiconductor die (col. 6, lines 12-19). A passivation layer 22 is applied over the front surface of semiconductor wafer 14, and a first passivation layer 24 is optionally applied immediately above passivation layer 22 (Fig. 2 and col. 6, lines 20-36). Openings are formed in passivation layer 24 over bond pads 18, 20, and redistribution traces 30 formed over passivation layer 24 electrically connect bond pads 18, 20 to laterally displaced solder bump pads 26 (col. 6, lines 62-68). Elenius et al. indicates that this arrangement accomplishes a redistribution of the typical conductive bond pads to a new pattern, such as an array distribution pattern (col. 7, lines 29-32). A second passivation layer 32 is formed over redistribution traces 30, and solder balls 28 are formed upon and attached to solder pads 26 exposed through passivation layers 24 and 32 (col. 8, line 5-19).

The Office Action indicates that Duboz teaches a metal connection 58 formed in the passivation layer which has been sized and configured to temporarily receive a substantially spherical interconnection element 67 attached to a semiconductor device 30. Page 3, paragraph 6.

Applicant proposes to amend independent claim 1 to recite, *inter alia*, "wherein the metal-lined via is sized and configured to temporarily establish an electrical connection by way

of biased contact with a substantially spherical interconnection element attached to a semiconductor device."

Applicant respectfully submits that no teaching or suggestion is found within Duboz for temporarily establishing an electrical connection by way of biased contact with a substantially spherical interconnection element attached to a semiconductor device.

Rather, Duboz teaches and suggests that "the silicon chips turned upside down are bonded via their front face to the front face of the main substrate 30, preferably by means of indium balls." Col. 4, lines 59-61. Applicant respectfully submits that Duboz teaches and suggests that the indium balls are melted between the silicon chips and the main substrate to bond and provide electrical communication therebetween. Similarly, Applicant respectfully submits that Schaefer et al. discloses that contact bump 212 is formed over under bump pad 210 using conventional solder bumping or balling techniques for subsequent reflow to a board contact on an external substrate 214 (col. 6, lines 44-45 and col. 7, lines 8-13). Further, Elenius et al. also teaches that a joint is formed between solder ball 28 and solder bump pad 26 (col. 8, lines 7-9).

Accordingly, Applicant respectfully asserts that the combination of Duboz, Schaefer, and Elenius does not teach or suggest all the claim limitations of independent claim 1, as proposed to be amended.

In addition, Applicant respectfully submits that one of ordinary skill in the art would not be motivated to combine the proposed references.

Specifically, Applicant respectfully asserts that one of ordinary skill in the art would not be motivated to combine the teachings of Schaefer with Duboz because each of the references relate to bonding of interconnection elements to a bond or contact pad, while independent claim 1 relates to a metal-lined via configured for biased contact against a substantially spherical interconnection element attached

Schaefer explains,

> "When the flip chip package's contact bumps are coupled with the PCB's pads, the die of the flip chip package typically has a substantially different coefficient of thermal expansion (CTE) than the PCB. This difference in CTE's causes the die and the PCB to expand and contract at different rates and to pull and push on the contact bumps package and results in deformation and stresses of the contact

> bumps. These stresses may ultimately result in damage to the flip chip package, such as solder joint fatigue. By way of another stress related problem, stresses introduced at the contact bump may cause the contact bump to push into the underlying layers that form the die and cause substantial craters within the die itself." Col. 2, lines 32-49.

Applicant respectfully submits that the stress-related detriments that are taught by Schaefer (and relied upon for motivation to combine the references cited in the rejection) develop, at least in part, in response to melting and bonding (i.e., reflowing or soldering) of the contact bump (i.e., solder ball) to a contact pad, followed by subsequent increases in temperature, as discussed in greater detail hereinbelow.

Accordingly, Applicant respectfully submits that because such stress related detriments taught by Schaefer relate to bonding of an interconnection element (e.g., a solder ball) to a contact pad, the motivation of eliminating such stresses is not tenable for supporting an obviousness rejection of independent claim 1, because independent claim 1, as proposed to be amended, distinguishes from bonding occurring between the metal-lined via and a substantially spherical interconnection element.

Put another way, because independent claim 1, as proposed to be amended, relates to a metal-lined via that is sized and configured to temporarily establish an electrical connection by way of biased contact with a substantially spherical interconnection element attached to a semiconductor device, one of ordinary skill in the art would not be motivated to combine any of Duboz, Schaefer, and Elenius, because the teachings of each of the references relates to bonding an interconnection element to a contact pad.

In addition, one of ordinary skill in the art would not make the proposed combination of Schaefer and Duboz because each reference teaches and suggests interconnection structures specifically suited for incongruous or generally opposite thermal stresses.

The Office Action states that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to make Duboz's metal connection in form of metal lined via to prevent stress related problems such as crate formations within the die as taught by Schafer and to provide the a conductive trace over a dielectric layer in Duboz in view of Schafer's invention in order to improved the chip scale package by providing a small form factor..." Pages 4-5, paragraph 7.

Applicant notes that the configuration proposed by Duboz relates to infrared detectors that are intended to "operate at very low temperatures (around 77 Kelvin)." Col. 1, lines 64-65. Therefore, Duboz teaches that "indium is chosen for its great capacity to absorb the stresses which are produced on going from room temperature to the very low use temperature." Col. 1, lines 65-66. Thus, Applicant respectfully asserts that Duboz teaches and suggests a bonded contact pad and interconnection element structure that is suited for the stresses associated with a reduction in temperature (i.e., contraction) following bonding of the contact pad and the interconnection element structure.

In contrast, Schaefer teaches and suggests that "stresses introduced at the contact bump may cause the contact bump to push into the underlying layers that form the die and cause substantial craters within the die itself." Col. 2, lines 45-49. Applicant respectfully submits that the bonded contact pad and interconnection element structure Schaefer teaches and suggests is directed toward stresses developed associated with an increase in temperature (i.e., expansion) following bonding of the contact pad and the interconnection element structure.

Accordingly, Applicant respectfully asserts that one of ordinary skill in the art would not be motivated to combine Duboz with Schaefer because each reference teaches bonded contact pad and interconnection element structures which are specifically tailored for generally opposite thermal stress conditions. Further, Applicant respectfully asserts that Duboz does not teach or suggest that its interconnection structure is suitable for the increases in temperature to which Schaefer is directed. Similarly, Applicant respectfully asserts that Schaefer does not teach or suggest that its interconnection structure is suitable for the decreases in temperature to which Duboz is directed.

Given the considerable differences between the structures of Duboz and Schaefer and the conditions for which each specifically pertains, Applicant respectfully submits that Duboz teaches away from combination with Schaefer and vice versa. Further, such modification may render each of the disparate structures unsatisfactory for its intended purpose, respectively. That is, modification of the Duboz structure according to the teachings of Schaefer may interfere with a capability of the Duboz structure to resist thermal stresses due to decreases in temperature and vice versa.

In summary, because the referenced do not teach or suggest all the claim limitations and

there is no motivation to combine the references, Applicant respectfully asserts that independent claim 1, as proposed to be amended, is allowable. Accordingly, Applicant respectfully requests reconsideration and allowance of independent claim 1, as proposed to be amended.

Also, each of dependent claims 2 through 4 and 6 through 11 is allowable as depending from independent claim 1, which is allowable. Applicant respectfully requests reconsideration and allowance of dependent claims 2 through 4 and 6 through 11.

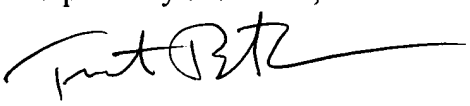
ENTRY OF AMENDMENTS

The proposed amendments to claims 1 through 4 and 6 through 11, the proposed amendments to withdrawn claims 5 and 12, and new claims 13 through 15, as presented hereinabove, should be entered by the Examiner because the proposed amendments and new claims are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments and new claims do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1 through 4, 6 through 11, and 13 through 15 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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